IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:	Edward R. Rhoads, et al.	§	Conf. No.:	8924
Serial No.:	10/764,617	§	Art Unit:	2185
Filed:	January 26, 2004	§	Examiner:	Zhuo H. Li
For:	Organizing Information Stored in Non-Volatile Re-Programmable Semiconductor Memories	§	Atty Docket:	ITL.0241D1US (P7376D)

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APPEAL BRIEF

Date of Deposit: February 23, 2010
I hereby certify that this document is being electronically transmitted on the date indicated above.

Khristine McNeil

TABLE OF CONTENTS

REAL PARTY IN INTEREST

The real party in interest is the assignee Intel Corporation.

RELATED APPEALS AND INTERFERENCES

Appeal No. 2008-2317, decision mailed November 21, 2008, attached in Related Proceedings Appendix.

STATUS OF CLAIMS

Claims 1-15 (Rejected).

Claims 16-25 (Canceled).

Claims 26-30 (Rejected).

Claims 1-15 and 26-30 are rejected and are the subject of this Appeal Brief.

STATUS OF AMENDMENTS

All amendments to the claims have been entered.

SUMMARY OF CLAIMED SUBJECT MATTER

In the following discussion, the independent claims are read on one of many possible embodiments without limiting the claims:

1. A method of organizing stored information comprising:

partitioning on a non-volatile, re-programmable semiconductor memory (Figure 2, 14) (Specification at page 4, lines 16-18) into a plurality of partitions, each having a defined address (Figure 5, 22) (Specification at page 11, lines 4-25); and

storing the defined address for one partition in another partition (Specification at page 15, lines 1-15).

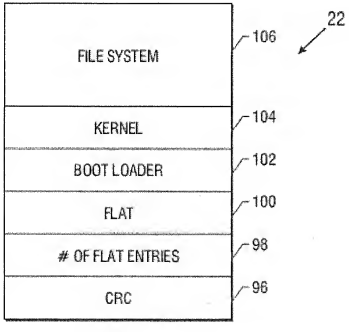

FIG. 5

10. A non-volatile, re-programmable semiconductor memory comprising:

a plurality of addressable partitions (Figure 6, 14), including a partition storing an operating system (Figure 5, 22); and

a storage location storing an address for one of said partitions in association with information about the information stored in said partition (Specification at page 11, lines 4-16, page 12, lines 1-6, and page 15, lines 1-15).

26. A processor-based system comprising:

a processor (Figure 6, 65);

a volatile memory (Figure 6, 68) coupled to said processor; and

a re-programmable, non-volatile semiconductor memory (Figure 5, 96, 98, 100, 102, 104, 106) coupled to said processor, said semiconductor memory including a plurality of partitions (Figure 6, 14), one of said partitions storing an operating system (Figure 5, 22) and another of said partitions (Figure 5, 102) storing the addresses of the other partitions in association with information about what is stored in each of said partitions (Specification at page 11, lines 4-16, page 12, lines 1-6, page 15, lines 1-15).

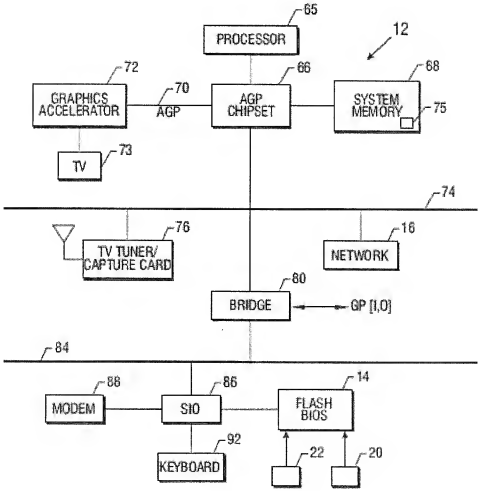

FIG. 6

At this point, no issue has been raised that would suggest that the words in the claims have any meaning other than their ordinary meanings. Nothing in this section should be taken as an indication that any claim term has a meaning other than its ordinary meaning.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. **Whether claims 1-15 and 26-30 are anticipated under 35 U.S.C. § 102(e) by Tallam (US 6,948,099).**

ARGUMENT

A. Are claims 1-15 and 26-30 anticipated under 35 U.S.C. § 102(e) by Tallam (US 6,948,099)?

The essence of the issue on this appeal is that a reference assigned to the assignee of the present application was prepared by the same patent attorney who prepared this application. In the course of preparing that reference application, the patent attorney used material from this present application in the cited reference application.

Thus, the prosecuting attorney knows that the material relied upon in the cited reference application is taken from the present application because it was he, the prosecuting attorney, who put the material in the reference application. Unfortunately, the reference application was filed first and is now applied as a § 102 rejection.

Incredibly, the Examiner now takes the position that the patent attorney's direct knowledge is for some reason insufficient to show derivation. Here, the only person who knows what happened is the prosecuting attorney who took the material from the present pending application during application preparation and put it into the cited reference application. Thus, there was no one else with personal knowledge of what happened. It is not reasonable to suggest that the one person in the world who has personal knowledge cannot explain why this happened and thereby show that the material in the cited reference was derived from the present applicants. As a result, the rejection should be reversed.

1. The argument that "Applicant failed to provide a satisfactory showing that the relevant portions of the patent originated with or were obtained from the instant application and that that subject matter is now claimed."

The Declaration, attached in the Evidence Appendix, is explicit that the material was obtained in the present application by the undersigned attorney who copied it from the previous application. Thus, there is no question but that the observation is incorrect.

2. The Applicant did not provide separate arguments with respect to art rejection of claims 1-15 and 26-30

No separate arguments are needed because the reliance on Tallam is misplaced. Since Tallam is not prior art, no further arguments are needed.

Therefore, the rejection should be reversed.

* * *

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date: February 23, 2010

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CLAIMS APPENDIX

The claims on appeal are:

1. A method of organizing stored information comprising:

partitioning on a non-volatile, re-programmable semiconductor memory into a plurality of partitions, each having a defined address; and

storing the defined address for one partition in another partition.

2. The method of claim 1 further including storing information about the number of partitions.

3. The method of claim 1 further including storing a boot loader in one of said partitions.

4. The method of claim 1 further including storing a file system in one of said partitions.

5. The method of claim 1 further including storing a kernel for an operating system in one of said partitions.

6. The method of claim 1 further including storing information in association with said addresses about whether or not an integrity check needs to be done on the data stored at the associated address.

7. The method of claim 1 further including storing, in association with the address of a partition, information about the type of information stored in the partition.

8. The method of claim 7 further including storing information about whether or not the information stored at a given partition is a boot loader, a kernel or a file system.

9. The method of claim 7 including storing information about the load address for said information in association with said address.

10. A non-volatile, re-programmable semiconductor memory comprising:

a plurality of addressable partitions, including a partition storing an operating system; and

a storage location storing an address for one of said partitions in association with information about the information stored in said partition.

11. The memory of claim 10 wherein said memory is a FLASH memory.

12. The memory of claim 10 wherein one of said partitions stores a basic input/output system.

13. The memory of claim 10 wherein one of said partitions stores a file system.

14. The memory of claim 10 wherein one of said partitions stores a kernel for an operating system.

15. The memory of claim 10 wherein one of said partitions stores a boot loader.

26. A processor-based system comprising:

a processor;

a volatile memory coupled to said processor; and

a re-programmable, non-volatile semiconductor memory coupled to said processor, said semiconductor memory including a plurality of partitions, one of said partitions storing an operating system and another of said partitions storing the addresses of the other partitions in association with information about what is stored in each of said partitions.

27. The system of claim 26 wherein said semiconductor memory is a FLASH memory.

28. The system of claim 26 wherein one of said partitions stores a basic input/output system.

29. The system of claim 26 wherein one of said partitions stores a file system.

30. The system of claim 26 wherein one of said partitions stores a boot loader.

EVIDENCE APPENDIX

Declaration by prosecuting attorney under 37 C.F.R. § 1.132 filed with Request for Continued Prosecution and Preliminary Amendment January 20, 2009.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:	Edward R. Rhoads et al.	§	Art Unit:	2185
		§		
		§	Examiner:	Zhuo H. Li
Serial No.:	10/764,617	§		
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		§		
		§	Assignee:	Intel Corporation

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DECLARATION UNDER 37 C.F.R. § 1.132 (ATTRIBUTION)

Sir:

The undersigned hereby states as follows:

1. I am the attorney who prosecuted both the pending application and the cited reference to Tallam.

2. A common disclosure was used as a matter of convenience for the two patent applications.

3. I obtained the material about putting the address for one section in another section including what is described in Figure 5 from inventors Rhoads and Ketrenos and put this material in the Tallam application. Thus, I was the person who put this information in the Tallam application. I obtained the information from Rhoads and Ketrenos.

4. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and, further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: January 20, 2009

Timothy N. Trop, Reg. No. 28,994

RELATED PROCEEDINGS APPENDIX

Appeal No. 2008-2317, decision mailed November 21, 2008.

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,617	01/26/2004	Edward R. Rhoads	ITL.0241D1US (P7376D)	8924

21906 7590 11/21/2008

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2185	

MAIL DATE	DELIVERY MODE
11/21/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte EDWARD R. RHOADS and JAMES P. KETRENOS

Appeal 2008-2317
Application 10/764,617[1]
Technology Center 2100

Decided: November 20, 2008

Before JOSEPH L. DIXON, JEAN R. HOMERE, and
ST. JOHN COURTENAY III, *Administrative Patent Judges*.

HOMERE, *Administrative Patent Judge*.

DECISION ON APPEAL

I. STATEMENT OF CASE

Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1 through 15 and 26 through 30. Claims 16 through 25 have been canceled. We have jurisdiction under 35 U.S.C. § 6(b). We affirm.

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[1] Filed on January 26, 2004. The real party in interest is Intel Corp.

The Invention

Appellants invented a method and system for organizing information stored in a non-volatile reprogrammable semiconductor memory. (Spec. 1.) As depicted in Figure 5, the memory is segmented into a plurality of partitions. (Spec., 11, ll. 4-25.) Each partition of the non-volatile reprogrammable memory has a defined address (22), which is stored in another partition of that same memory device. (*Id.* 15, ll. 1-15.)

Representative Claim

Independent claim 1 further illustrates the invention. It reads as follows:

1. A method of organizing stored information on a non-volatile, re-programmable semiconductor memory comprising:

partitioning said memory into a plurality of partitions, each having a defined address; and

storing the defined address for one partition in another partition.

Prior Art Relied Upon

The Examiner relies on the following prior art as evidence of unpatentability:

Bunnell	US 5,594,903	Jan. 14, 1997
Tallam	US 6,948,099 B1	Sep. 20, 2005 (filed Jul. 30, 1999)

Rejections on Appeal

The Examiner rejects the claims on appeal as follows:

A. Claims 1 through 15 and 26 through 30 stand rejected under non-statutory obviousness-type double patenting over claims 1 through 8 Tallam.

B. Claims 1 through 15 and 26 through 30 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Tallam.

C. Claims 1 through 15 and 26 through 30 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Bunnell.

Appellants' Contentions

1. Appellants argue that Tallam's claims do not teach storing a defined address for one partition in another partition, as recited in independent claim 1. (App. Br. 10-11, Reply Br. 1-2.) Therefore, Appellants submit that Tallam's claims cannot be properly relied upon to reject the claimed invention under non-statutory obviousness-type double patenting. (*Id.*)

2. Appellants argue that while Tallam's Specification discloses the limitation of storing the defined address of one partition into another partition, such limitation was neither invented nor claimed by Tallam. (*Id.*) As detailed in the declaration submitted by Appellants' representative under 37 C.F.R. § 1.132, Appellants contend that they invented the claimed limitation prior to the filing date of the Tallam application for patent. (*Id.*)

Further, they assert that during the drafting of the Tallam application, the cited material was derived from inventors Rhoads and Ketrenos. (*Id.*) Therefore, Appellants submit that the disclosure of the Tallam patent cannot be properly relied upon to reject the claimed invention under anticipation.

3. Appellants argue that Bunnell does not teach a non-volatile reprogrammable semiconductor memory wherein the defined address of one partition is stored in another partition, as recited in independent claim 1. (Appeal Br. 12-13, Reply Br. 3-4.) Therefore, Appellants submit that Bunnell does not anticipate the claimed invention. (*Id.*)

Examiner's Findings

1. The Examiner finds that, as recited in claim 2 of the Tallam patent, the second portion for storing a recovery operating system and instructions to obtain an outside operating system substantially teaches the claimed limitation recited in Appellants' claim 10. (Ans. 11-12.) The Examiner therefore concludes that Tallam's claims render Appellants' claims unpatentable under non-statutory obviousness double patenting. (*Id.*)

2. The Examiner finds that the declaration submitted by Appellants' representative to be insufficient to show that Appellants invented the claimed limitation prior to the filing date of the Tallam application for patent. (*Id.* 12-13.) Therefore, the Examiner maintains that Tallam anticipates the claimed invention. (*Id.*)

3. The Examiner finds that Bunnell's disclosure of a virtual memory having a nonvolatile portion implemented as an EPROM or EEPROM that uses headers to provide address of a data segment to a corresponding code segment in an alterable portion of the memory teaches the claimed limitations. (*Id.* 14-15.) Therefore, the Examiner maintains that Bunnell anticipates the claimed invention. (*Id.*)

II. ISSUES

1. Have Appellants shown that the Examiner erred in concluding that the second portion for storing a recovery operating system and instructions, as recited in claim 2 of the Tallam patent, renders Appellants' claimed invention unpatentable under non-statutory obviousness double patenting? We answer this inquiry in the affirmative.

2. Have Appellants shown that the Examiner erred in finding that Tallam's disclosure of storing the address of a partition in another partition antedates Appellants' claimed invention? We answer this inquiry in the negative.

3. Have Appellants shown that the Examiner erred in finding that Bunnell's disclosure of a memory space having a ROM and a RAM wherein the ROM uses headers to access address information and copy data in the RAM teaches the claimed invention? We answer this inquiry in the affirmative.

FINDINGS OF FACT

The following findings of fact (FF) are supported by a preponderance of the evidence.

Appellants' Admission

Appellants confirm the following:

1. Appellants' representative, Mr. Timothy Trop, drafted both the Application on appeal and that of the Tallam patent. (App. Br.10.)

2. As a matter of convenience, Mr. Trop utilized in the two applications for patent a common Specification combining the two separate inventions. (*Id.*)

3. Mr. Trop filed a declaration under 37 C.F.R. § 1.1.32 to show that the claimed material pertaining to storing the defined address for one partition into another partition is attributed to Appellants pursuant to MPEP 716.10. Particularly, the declaration indicates that, while the cited subject matter is disclosed in the Specification of the Tallam patent, it was neither invented nor claimed by Tallam. Rather, it was invented and claimed by Rhoads and Ketrenos of the present application. (*Id.*)

Tallam

4. As depicted in Figure 5, Tallam discloses a memory partitioned into a plurality of segments, each having a defined address (22). (Col. 4, ll. 59-67.)

5. As shown in Figure 7, Tallam discloses storing the defined address for one partition in another partition. (Col. 6, ll. 24-38.)

6. Tallam's claims recite a FLASH memory having a plurality of partitions, wherein a first partition stores a primary operating system, and wherein a second partition stores a recovery operating system and instructions to obtain a new operating system outside of the memory. (Col. 8, ll. 9-48.)

Bunnell

7. As depicted in Figure 3, Bunnell discloses a main memory (14) having a virtual address space portion (60) including a non-volatile ROM segment (62), which is implemented using a combination of ROM, EPROM, EEPROM and flash EPROM storage devices. The virtual storage device (60) further includes an alterable portion of memory (64) implemented as a RAM. (Col. 7, ll. 41-52.)

8. For each application program to be executed, Bunnell discloses storing in the ROM a plurality of address headers and data segments associated with the program. Bunnell also discloses storing in the RAM code segments (116, 118, 120, 122) corresponding to the data segments for the program. To execute the application program, the headers provide the address of the corresponding code segments to the data segments (Col. 10, l. 35- col. 1. 24.)

PRINCIPLES OF LAW

35 U.S.C. § 101

Double Patenting

The doctrine of double patenting seeks to prevent the unjustified extension of patent exclusivity beyond the term of a patent. The public policy behind this doctrine is that:

> The public should . . . be able to act on the assumption that upon the expiration of the patent it will be free to use not only the invention claimed in the patent but also any modifications or variants thereof which would have been obvious to those of ordinary skill in the art at the time the invention was made, taking into account the skill in the art and prior art other than the invention claimed in the issued patent.

In re Zickendraht, 319 F.2d 225, 232 (CCPA 1963) (Rich, J., concurring).

Double patenting results when the right to exclude granted by a first patent is unjustly extended by the grant of a later issued patent or patents. *In re Van Ornum*, 686 F.2d 937 (CCPA 1982).

ANTICIPATION

In rejecting claims under 35 U.S.C. § 102, "[a] single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation." *Perricone v. Medicis Pharmaceutical Corp.*, 432 F.3d 1368, 1375 (Fed. Cir. 2005), citing *Minn. Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 1565 (Fed. Cir. 1992). "Anticipation of a patent claim requires a

finding that the claim at issue 'reads on' a prior art reference." *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed Cir. 1999) ("In other words, if granting patent protection on the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is anticipated, regardless of whether it also covers subject matter not in the prior art.") (internal citations omitted).

DERIVATION

When the unclaimed subject matter of a patent, application publication, or other publication is applicant's own invention, a rejection, which is not a statutory bar, on that patent or publication may be removed by *submission of evidence* establishing the fact that the patentee, applicant of the published application, or author derived his or her knowledge of the relevant subject matter from applicant. Moreover applicant must further show that he or she made the invention upon which the relevant disclosure in the patent, application publication, or other publication is based. *In re Mathews*, 408 F.2d 1393 (CCPA 1969); *In re Facius*, 408 F.2d 1396 (CCPA 1969). See MPEP 715.01(c)

ATTRIBUTION

When subject matter, disclosed but not claimed in a patent application filed jointly by S and another, is claimed in a later application filed by S, the joint patent or joint patent application publication is a valid reference

available as prior art under 35 U.S.C. § 102(a), (e), or (f) unless overcome by affidavit or declaration under 37 C.F.R. § 1.131 showing prior invention (see MPEP § 715) or *an unequivocal declaration* by S under 37 C.F.R. § 1.132 that he or she conceived or invented the subject matter disclosed in the patent or published application... However, it is incumbent upon *the inventors named in the application, in response to an inquiry regarding the appropriate inventorship under 35 U.S.C. § 102(f) or to rebut a rejection under 35 U.S.C. § 102(a) or (e), to provide a satisfactory showing by way of affidavit under 37 C.F.R. § 1.132 that the inventorship of the application is correct in that the reference discloses subject matter derived from the applicant rather than invented by the author, patentee, or applicant of the published application notwithstanding the authorship of the article or the inventorship of the patent or published application. In re Katz*, 687 F.2d 450, 455 (CCPA 1982) (inquiry is appropriate to clarify any ambiguity created by an article regarding inventorship and it is then incumbent upon the applicant to provide "a satisfactory showing that would lead to a reasonable conclusion that [applicant] is the ... inventor" of the subject matter disclosed in the article and claimed in the application). See MPEP § 716.10.

ANALYSIS

35 U.S.C. § 101

As set forth in the Findings of Fact section, Tallam's claims recite a reprogrammable semiconductor memory having a plurality of partitions for

storing different operating systems. (FF. 6.) We fail to find any teaching in the cited claims pertaining to storing the address of one partition in another partition. We agree with Appellants that the Examiner improperly relied upon non-claimed subject matter disclosed in the detailed description of the Tallam patent, as evidence of the state of the prior art. We therefore, conclude that one of ordinary skill in the art would not have combined subject matter disclosed in the detailed description and the claim of the cited patent to render the claimed invention unpatentable under obviousness-type double patenting. It follows that Appellants have shown that the Examiner erred in concluding that Tallam renders the claimed invention unpatentable under obviousness-type double patenting. We therefore, will not sustain the Examiner's rejection of claims 1 through 15 and 26 through 30 as being unpatentable under obviousness-type double patenting.

35 U.S.C. § 102

1. Tallam

As set forth in the Findings of Facts, Appellants' representative submits a declaration under 37 C.F.R. § 1.132 to show that the subject matter pertaining to storing the address of a partition in another partition of a non-volatile reprogrammable memory was invented by Appellants, and not Tallam. (FF. 1-3.) We agree with the Examiner that the submitted declaration is insufficient to show that the claimed subject matter is either attributed to or derived from Appellants. Firstly, the declaration is improper

to show that the claimed subject matter is attributed to Appellants since they did not jointly file the present application with Tallam's. Therefore, attribution is not germane to this case. Secondly, the declaration is insufficient to show that the invention was derived from Appellants since it fails to prove that Appellants invented the claimed subject matter. Particularly, the submitted declaration merely provides a conclusory statement by Appellants' representative to suggest that the cited subject matter was invented by Appellants and not Tallam. We note however that such gratuitous statement, without any supporting evidence to show the actual descriptions or statements of the inventions that the representative received from each of the respective inventive entities before combining the inventions into one, is not persuasive. While the declarations and the exhibits are in the form of testimonial and corroborating evidence, arguments of counsel are not evidence. See, e.g., *Meitzner v. Mindick*, 549 F.2d 775, 782 (CCPA 1977); *In re Pearson*, 494 F.2d 1399, 1405 (CCPA 1974). It follows that Appellants have not shown that the Examiner erred in finding that Tallam anticipates independent claim 1. Therefore, we will sustain the rejection of independent claim 1.

Appellants did not provide separate arguments with respect to the rejection of claims 1 through 15 and 26 through 30. Therefore, we select independent claim 1 as being representative of the cited claims. Consequently, claims 2 through 15 and 26 through 30 fall together with representative claim 1. 37 C.F.R. § 41.37(c)(1)(vii).

2. Bunnell

As set forth in the Findings of Fact section, Bunnell discloses a virtual memory space having a non-volatile reprogrammable ROM and an erasable RAM. Particularly, Bunnell discloses using headers to communicate addresses of data segments in the ROM with corresponding code segments in the RAM during the execution of an application program. (FF. 7-8.) While Bunnell teaches that the ROM is a non-volatile and reprogrammable memory (i.e., implemented through EEPROM) having headers to copy data into a RAM during execution of the program, it does not teach that storing the address of one partition of the non-volatile/reprogrammable memory into another partition of said memory. Rather, it teaches storing data (not address) from a segment of the non-volatile programmable ROM to another segment of the erasable RAM. We thus agree with Appellants that Bunnell does not reasonably teach the claimed limitation. It follows that Appellants have shown that the Examiner erred in finding that Bunnell anticipates claim 1. Because claims 2 through 15 and 26 through 30 recites these same limitations, we will not sustain the Examiner's rejection of claims 1 through 15 and 26 through 30 as being anticipated by Bunnell.

CONCLUSIONS OF LAW

A. Appellants have shown that the Examiner erred in finding that:

1. Tallam renders claims 1 through 15 and 26 through 30 unpatentable under non-statutory obviousness-type double patenting.

2. Bunnell anticipates claims 1 through 15 and 26 through 30 under 35 U.S.C. § 102(b).

We reverse these rejections

B. Appellants have not shown that the Examiner erred in finding that Tallam anticipates claims 1 through 15 and 26 through 30 under 35 U.S.C. § 102(e). We affirm this rejection.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

rwk

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